## REMARKS

The amendment of claims 3 and 20 are made to correct typographical errors and are not made in response to the Examiners rejection of claims 3 and 20.

The Examiner rejected claims 1-20 under 35 U.S.C. 103(a) as being unpatentable over Yamagata (US 5,319,589) in view of Murakami (US 5,134,585).

Applicants respectfully traverse the §103(a) rejections with the following arguments.

**35 USC § 103 Rejections**

As to claims 1-20, the Examiner states that "Yamagata discloses a content-addressable memory with bitline replacement that uses a non-adjacent spare adjacent bitline. Referring to Fig. 16 of Yamagata, a 'coupling circuit' 10 for coupling bitlines (DTO-DT35, DTS), and their complements, to data lines (100-1035) is controlled by a 'steering signal' (400-435) for each data line. Yamagata's 'coupling circuit', in operation, 'couples (to) a first respective bitline or to a second respective bitline based on a steering signal', however Yamagata's "first bitline" and the replacement 'second bitline' (DTS) are non-adjacent, except in the case of one bitline (DT35). Yamagata further shows a circuit (500-535, 5S) that 'maintains said first respective bitline at a desired potential after said data line is coupled to said second bitline' so that a faulty unselected bitline does not introduce noise in reading. Yamagata's bitline coupling selection signals (NED) are controlled (Fig. 18) by a combination of fuse (46) and latch (47), thereby providing 'fuse latches'. Murakami discloses a memory array with bitline replacement using adjacent bitlines (Fig. 8), which is a well-known functional equivalent alternative to using a non-adjacent spare bitline for bitline replacement. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Yamagata's memory chip by replacing the non-adjacent bitline sparing with Murakami's adjacent bitline sparing. Such a substitution would have been obvious because Murakami's adjacent bitline sparing was already a well-known functional equivalent alternative. Regarding claims 4 and 13, for inverted bitlines (DT/0-DT/35), the 'desired potential is ground'."

First, Applicants respectfully contend it is impossible to replace the switching network of Yamagata et al. with the switching network of Murkami et al. The switching network of Yamagata et al. is taught as using data lines connected to different bitlines, but the switching

network of Murkami et al. is taught as using one data line connected to multiple bitlines. Applicants see no teaching in either Yamagata et al. or Murkami et al. nor has the Examiner provided any reference teaching how to resolve this contradiction.

Second, Applicants respectfully contend, if it were possible to modify Yamagata et al. with Murkami et al, that replacing the switching network of Yamagata et al. with the switching network of Murkami et al, destroys the function of Yamagata et al. The switching network of Yamagata et al. allows any input data line DT01-DT35 to be replaced by redundant input data line DTS. Replacing the switching network of Yamagata et al. with the switching network of Murkami et al. would only allow DT35 to be replaced by redundant input data line DTS.

Third, Applicants respectfully contend that Yamagata et al. teaches away from the Examiners combination of Yamagata et al. with Murkami et al. as the goal of Yamagata et al. as stated in col. 4, lines 5-11 is: " Another object of the present invention is to implement a dynamic content addressable memory device by simplified circuit configuration. Still another object of the present invention is to provide a dynamic content addressable memory operating under simplified control." Yamagata et al. requires only one input data line be switched in response to a single failed memory cell, while the modification of Yamagata by Murkami et al. requires multiple lines to be switched in response to a single failed memory cell which in turn requires a vastly more complicated switching network and corresponding control circuits in direct opposition to the stated goals of Yamagata et al.

Fourth, Applicants respectfully request the Examiner provide evidence of the Examiners assertion that "bitline replacement using adjacent bitlines (Fig. 8), which is a well-known functional equivalent alternative to using a non-adjacent spare bitline for bitline replacement" under MPEP 2144.03C. Applicants respectfully contend that since Yamakata et al. teaches a

content addressable memory and Murkami et al. teaches a random access memory, each having different read and write requirements and it therefore not obvious to take a sparing technique taught for random access memory and apply it to a content addressable memory.

Based on the preceding arguments, Applicants respectfully maintain that claims 1, 9 and 17 are not unpatentable over Yamagata et al. in view of Murkami et al and are in condition for allowance. Since claims 2-8 depend from claim 1, claims 10-16 depend from claim 9 and claims 18-20 depend from claim 17, Applicants respectfully maintain that claims 2-8, 10-16 and 18-20 are likewise in condition for allowance.

Applicants respectfully contend that claim 17 is not obvious in view of view of Yamagata et al. in view of Murakami et al. because view of Yamagata et al. in view of Murakami et al. does not teach or suggest every feature of claim 17. For example, Yamagata et al. in view of Murakami et al. does not teach or suggest "means for directing a first respective read line coupled to said first respective bitline to a second respective read line coupled to said second respective bitline in response to said steering signal." Applicants respectfully point out that Yamagata et al. is silent as to redirection of read lines (and Murakami et al. does not use read lines).

## CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invite the Examiner to contact the Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0456.

Respectfully submitted,
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